|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | EnSp | RegWriteEn | RS/Im/RD | RD/Sp | Branch/SLL | ALUop | Cin | Ainv | Binv | MemToReg | Branch | Load | Store | Input | Output | DspEn |
| Add | 0 | 1 | 00 | 0 | 0 | 000 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Addi | 0 | 1 | 01 | 0 | 0 | 000 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Sub | 0 | 1 | 00 | 0 | 0 | 001 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Sll | 1 | 1 | 01 | 1 | 1 | 010 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| And | 0 | 1 | 00 | 0 | 0 | 011 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Nand | 0 | 1 | 00 | 0 | 0 | 100 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Lw | 1 | 1 | 01 | 1 | 0 | XXX | X | X | X | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| Sw | 1 | 0 | 01 | 1 | 0 | XXX | X | X | X | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| Beq | 1 | 0 | 10 | 1 | 1 | 101 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| Slt | 1 | 0 | 00 | 1 | 0 | 110 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| jmp | 0 | 0 | 10 | X | 0 | XXX | X | 0 | X | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| inp | 0 | 1 | 00 | 0 | 0 | XXX | X | X | X | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| otp | 0 | 0 | 00 | 0 | 0 | XXX | X | X | X | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Dsp | 0 | 0 | 00 | 0 | 0 | XXX | X | X | X | 0 | 0 | 0 | 0 | 0 | 1 | 1 |